CLAIMS

What is claimed is:

1. A method of producing an integrated circuit (IC) device layout corresponding to an IC device design, said method comprising:

(a) generating an initial layout corresponding to the IC device design, said initial layout complying with a predetermined set of design rules;

(b) simulating how structures within the initial layout will pattern on a wafer;

(c) identifying portions of the simulated layout which demonstrate poor manufacturability; and

(d) creating at least one design rule to disallow at least one portion of the layout identified in step (c).

2. The method of claim 1, said method further comprising:

(e) producing a layout complying with the design rules created at step (d); and

(f) simulating how structures within the layout produced at step (e) will pattern on a wafer.

3. The method of claim 2, said method further comprising:

repeating steps (c) - (f) until no portions of the simulated layout demonstrate poor manufacturability.

4. The method of claim 1, said method further comprising:

modifying at least one design rule of the predetermined set of design rules to disallow a portion of the layout identified in step (c).

5. The method of claim 1, said method further comprising:

performing at least one optical proximity correction (OPC) on the layout before performing step (b).

6. The method of claim 1, wherein step (c) includes performing optical rule checking (ORC) on the simulated layout.

7. The method of claim 6, wherein performing ORC includes checking at least one of aerial image metrics, resist image metrics, and post exposure bake metrics.

8. The method of claim 7, wherein the aerial image metrics include at least one of image log slope, contrast, minimum intensity, maximum intensity, and intensity at a given distance.

9. The method of claim 1, said method further comprising:

providing a graphical representation indicating layouts identified in step (c).

10. The method of claim 1, wherein the initial layout is embodied in a layout data file.

11. A method of producing design rules, said method comprising:

generating a plurality of parametrically varying layout patterns;

simulating how each layout pattern will pattern on a wafer;

classifying edges of structures within the simulated layout patterns based on manufacturability; and

creating design rules to disallow layout patterns demonstrating poor manufacturability.

12. The method of claim 11, wherein step (a) includes:

selecting at least one layout test pattern;

generating a design spreadsheet, said design spreadsheet including a plurality of parametrically varying design parameters; and

generating a plurality of layout data files from the design spreadsheet and the layout test pattern.

13. The method of claim 12, wherein the varying design parameters include at least one of pitch, linewidth, tip-to-tip distance, tip-to-line distance, and length.

14. The method of claim 11, said method further comprising:

performing at least one optical proximity correction (OPC) on the geometric layouts prior to the simulating step.

15. The method of claim 11, wherein step (c) includes performing optical rule checking (ORC) on edges of structures within the simulated layout patterns.

16. The method of claim 15, wherein performing ORC includes checking at least one of aerial image metrics, resist image metrics, and post exposure bake metrics.

17. The method of claim 16, wherein the aerial image metrics include at least one of image log slope, contrast, minimum intensity, maximum intensity, and intensity at a given distance.

18. The method of claim 11, said method further comprising:

providing a graphical representation of the plurality of parametrically varying layout patterns, said graphical representation being indicative of layout patterns that fail at least one ORC demonstrating good and poor manufacturability.

19. The method of claim 18, wherein the graphical representation includes a plurality of identifiers which correspond to one or more layout patterns having a combination of at least two design parameters.

20. A method of generating a set of design rules for a next generation technology, said method comprising:

(a) providing a design library of layout patterns corresponding to a current technology;

(b) scaling one or more layout patterns of the design library to the next generation technology;

(c) generating simulation images of the scaled layout patterns from step (b)

(d) performing optical rule checks (ORCs) on the simulation images from step (c);

(e) identifying layout patterns which fail one or more ORCs; and

(f) creating one or more design rules to disallow the layout patterns identified in step (e).

21. The method of claim 20, wherein the step of performing ORCs includes checking at least one of edge intensity slope, maximum intensity, minimum intensity, contrast and critical dimension control for structures within the simulation images.

22. The method of claim 20, said method further comprising:

modifying at least one pre-existing design rule from the current technology to disallow a layout pattern identified in step (e).